UNITED STATES PATENT AND TRADEMARK OFFICE

A

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/908,948	07/19/2001	Kenneth P. Parker	10001121-1	1925

7590 08/17/2005

AGILENT TECHNOLOGIES, INC.
Legal Department, DL429
Intellectual Property Administration
P. O. Box 7599
Loveland, CO 80537-0599

EXAMINER	
ABRAHAM, ESAW T	

ART UNIT	PAPER NUMBER
2133	

DATE MAILED: 08/17/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/908,948	PARKER, KENNETH P.	
	Examiner	Art Unit	
	Esaw T. Abraham	2133	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *24 June 2005*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *21-23* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☒ Claim(s) *1-20* is/are allowed.

6)☒ Claim(s) *21-23* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *19 July 2001* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

Response to the applicant's amendments

Applicant's argument, see appeal brief pages 10-17 filed on 06/24/2005 for claims 1-23 have been fully considered and are persuasive. Therefore, the final rejection made on 12/21/04 has been withdrawn. Claims 1-20 are allowed. However, upon further consideration, a new ground(s) of rejection for claim 21-23 is made in view of Naffziger (U.S. PN: 6,606,720)

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

The factual inquiries set forth in *Graham* **v.** *John Deere Co.*, 383 U.S. 1, 148 USPQ 459 (1966), that are applied for establishing a background for determining obviousness under 35 U.S.C. 103(a) are summarized as follows:

1. Determining the scope and contents of the prior art.
2. Ascertaining the differences between the prior art and the claims at issue.
3. Resolving the level of ordinary skill in the pertinent art.
4. Considering objective evidence present in the application indicating obviousness or nonobviousness.

1. Claims **21-23** are rejected under 35 U.S.C. 103(a) as being unpatentable over Wu (U.S. PN: 5,831,992) in view of Naffziger (U.S. PN: 6,606,720).

As per claims **21-23,** Wu teach in figure 1 disclosed functional elements including pattern generator (12), which is capable of generating a plurality of pseudo-random test vectors whereby

the functional elements (Scan chain 1 to Scan chain m) represent the circuit components within the circuit under test (CUT) for which fault diagnosis is required (see col. 4, lines 43-53). Wu further teach that all the scan chains are tested at the same time, and the test responses from all the scan chains are analyzed in parallel and when the scan chain fails an approach is to treat the multiple scan chains as multiple single scan chains, i.e., diagnose one chain at a time or in other words, the entire test set is applied to all the scan chains, but the test response from only a single chain is analyzed by gating the scan-out data (see in figure 2) and the controller (see element 18) is used to select the test responses (see col. 6, lines 45-59). Wu **does not explicitly** teach that the scan chains are out-of-phase. **However,** Naffziger in an analogous art teaches a method and apparatus for scanning data into and out of a latch and the method to reduce the transistor count for scan chain link (see col. 2, lines 33-43). Further, Naffziger teach that the scan chain link 308 which is associated with the latch 302 comprises first and second transfer gates 422/424, 426/428, a shift input, and an output inverting buffer 432 and each transfer gate 422/424, 426/428 comprises an NFET 422 and a PFET 424 which are connected in parallel via the sources and drains of each and the two transfer gates 422/424, 426/428 are opened and closed out of phase (i.e., in an alternating manner) (see col. 5, lines 8-29). **Therefore,** it would have been obvious to a person having an ordinary skill in the art at the time the invention was made to implement the teachings of Wu to include scan chains to employ out-of-phase operation as taught by Naffziger. **This modification** would have been obvious because a person Having ordinary skill in the art would have been motivated in order to allow a single periodic shift signal to fully control operation of the scan chain link and to reduce the transistor count of a non-wiggle scan chain link with an need for only two control signals (see col. 2, lines 40-42)

Examiner's statement for reason for allowance

2. Claims **1-20** have been allowed.

The following is an examiner's statement for allowance:

As per claim 1:

The prior art taken singly or in combination fail to teach, anticipate, suggest, or render obvious a current surge minimization circuitry which is interconnected with said plurality of interconnected circuit elements, whereby operation of said current surge minimization circuitry during operation of said number of scan chains minimizes current surges in said integrated circuit. Consequently, claim 1 is allowed over the prior art.

Claims **2-8,** which is/are directly or indirectly dependent/s of claim 1 are also allowable over the prior art of record.

As per claim 9:

The prior art taken singly or in combination fail to teach, anticipate, suggest, or render obvious means for minimizing current surges in said integrated circuit as said number of scan chains shift test data into and out of said plurality of interconnected circuit element. Consequently, claim 9 is allowed over the prior art.

Claims **10-11,** which is/are directly or indirectly dependent/s of claim 9 are also allowable over the prior art of record.

As per claim 12:

The prior art taken singly or in combination fail to teach, anticipate, suggest, or render obvious computer readable program code stored on the number of computer readable media, the

computer readable program code comprising program code for reading a circuit description file, the circuit description file comprising data which specifies current surge minimization file, at least some of said current surge minimization constraints being defined for operation of the circuit during operation of at least one scan chain of the circuit; rules and design elements for minimizing current surges in a circuit; and program code for synthesizing current surge minimization circuitry using said design elements, in conformance with said current surge minimization constraints and said rules for minimizing current surges in a circuit. Consequently, claim 12 is allowed over the prior art.

Claim 13, which is/are directly or indirectly dependent/s of claim 12 are also allowable over the prior art of record.

As per claim 14:

The prior art taken singly or in combination fail to teach, anticipate, suggest, or render obvious providing the integrated circuit with current surge minimization circuitry to be operated during operation of said number of scan chains. Consequently, claim 14 is allowed over the prior art.

Claims **15-20,** which is/are directly or indirectly dependent/s of claim 14 are also allowable over the prior art of record.

Conclusion

3. Any inquiry concerning this communication or earlier communication from the examiner should be directed to Esaw Abraham whose telephone number is (571) 272-3812. The examiner can normally be reached on M-F 8-5.

If attempts to reach the examiner by telephone are successful, the examiner's supervisor, Albert DeCady can be reached on (571) 272-3819. The fax phone numbers for the organization where this application or proceeding is assigned are (571) 273-8300 for regular communications and (571) 273-8300 for after final communications.

Information regarding the status of an Application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or PUBLIC PAIR. Status information for unpublished applications is available through Private Pair only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Esaw Abraham

Esaw Abraham

Art unit: 2133

ALBERT DECADY
SUPERVISORY PATENT EXAMINER
TECHNOLOGY CENTER 2100